37. The method of claim 36, wherein the n-typed impurities self-activate due to the excitation of the impurity particles.

38. The method of claim 35, wherein the impurity region is formed by heavily doping the region with p-typed impurities.

39. A thin film transistor prepared by a process comprising the steps of forming a gate insulating layer on an active layer; forming a gate on the gate insulating layer; forming an excited region in an exposed portion of the active layer by implanting hydrogen ions to the active layer while using the gate as a mask; and forming an impurity region by heavily implanting impurity ions to the excited region while the excited region remains in an excited state.

40. The thin film transistor of claim 39, wherein the gate insulating layer is formed by depositing silicon dioxide or silicon nitride on a glass substrate, and the active layer is formed by depositing polycrystalline silicon.

Please **WITHDRAW** Claims 1-20 from consideration after adding Claims 21-40.

REMARKS

Claims 1-20 are withdrawn from consideration while new Claims 21-40 are added. Examination and consideration of the application, as amended, are respectfully requested.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete

the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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